EXPRESS MAIL LABEL NO. EV381146372US

WHAT IS CLAIMED IS:

1. A differential non-volatile memory device comprising:

at least first and second OTP memory cells that are each coupled between a supply voltage and a reference voltage, the first and second memory cells being programmed to store a bit and its complementary bit;

a read circuit forming a first current path between the first memory cell and the reference voltage and a second current path between the second memory cell and the reference voltage for reading the bit and the complementary bit that are stored in the first and second memory cells, the first current path including a first circuit point that is associated with a first output terminal, and the second current path including a second circuit point that is associated with a second output terminal; and

setting means that can be activated to bring the first and second circuit points to a voltage value that is substantially equal to the reference voltage, the setting means being able to set the value of the current flowing through each of the first and second current paths.

2. The memory device according to claim 1, wherein the setting means comprises a current mirror that includes:

a current reference;

at least one first transistor coupled to the current reference; and

at least two second transistors, each of the second transistors being in one of the first and second current paths.

3. The memory device according to claim 1, further comprising first and second buffers, the first buffer being coupled between the first circuit point and the first output terminal, and the second buffer being coupled between the second circuit point and the second output terminal.

4. The memory device according to claim 1, further comprising a device coupled to the first and second circuit points for amplifying a voltage difference between the first and second circuit points after inactivation of the setting means.

5. The memory device according to claim 1, wherein the reference voltage is ground.

6. The memory device according to claim 1, further comprising a control circuit for activating setting means, and then inactivating the setting means and bringing one of the first and second circuit points to about the supply voltage and maintaining the other of the first and second circuit points at about the reference voltage.

7. An information processing system that includes at least one differential non-volatile memory device, the memory device comprising:

at least first and second OTP memory cells that are each coupled between a supply voltage and a reference voltage, the first and second memory cells being programmed to store a bit and its complementary bit;

a read circuit forming a first current path between the first memory cell and the reference voltage and a second current path between the second memory cell and the reference voltage for reading the bit and the complementary bit that are stored in the first and second memory cells, the first current path including a first circuit point that is associated with a first output terminal, and the second current path including a second circuit point that is associated with a second output terminal; and

setting means that can be activated to bring the first and second circuit points to a voltage value that is substantially equal to the reference voltage, the setting means being able to set the value of the current flowing through each of the first and second current paths.

8. The information processing system according to claim 7, wherein the setting means of the memory device comprises a current mirror that includes:

a current reference;

at least one first transistor coupled to the current reference; and

at least two second transistors, each of the second transistors being in one of the first and second current paths.

9. The information processing system according to claim 7, wherein the memory device further comprises first and second buffers, the first buffer being coupled between the first circuit point and the first output terminal, and the second buffer being coupled between the second circuit point and the second output terminal.

10. The information processing system according to claim 7, wherein the memory device further comprises a device coupled to the first and second circuit points for amplifying a voltage difference between the first and second circuit points after inactivation of the setting means.

11. The information processing system according to claim 7, wherein the reference voltage is ground.

12. The information processing system according to claim 7, wherein the memory device further comprises a control circuit for activating setting means, and then inactivating the setting means and bringing one of the first and second circuit points to about the supply voltage and maintaining the other of the first and second circuit points at about the reference voltage.

13. A method for reading a differential non-volatile memory device, the memory device including:

at least first and second OTP memory cells that are each coupled between a supply voltage and a reference voltage, the first and second memory cells being programmed to store a bit and its complementary bit; and

a read circuit forming a first current path between the first memory cell and the reference voltage and a second current path between the second memory cell and the reference voltage for reading the bit and the complementary bit that are stored in the first and second memory cells, the first current path including a first circuit point that is associated with a first output terminal and the second current path including a second circuit point that is associated with a second output terminal,

the method comprising the step of:

bringing the first and second circuit points to about the reference voltage, and setting a current flowing through each of the first and the second current paths so as to control the currents flowing through the first and second current paths; and

subsequently bringing one of the first and second circuit points to about the supply voltage and maintaining the other of the first and second circuit points at about the reference voltage.

14. The method according to claim 13, further comprising the step of:

after the step of subsequently bringing one of the first and second circuit points to about the supply voltage, buffering voltages at the first and second circuit points so as to provide output signals comprising the bit and the complementary bit.

15. The method according to claim 13, wherein in the step of the subsequently bringing one of the first and second circuit points to about the supply voltage, a voltage difference between the first and second circuit points is amplified.

16. The method according to claim 13, wherein the reference voltage is ground.